CLAIM LISTING

1. (Previously Presented) A method for managing bursts of data, the method comprising:

storing data in a machine readable memory device a first time at a first memory address;

the machine readable memory device having two or more burst boundaries; and

the first memory address having a first alignment with respect to the burst boundaries;

storing the data in the machine readable memory device a second time at a second memory address, the second memory address having a second alignment with respect to the burst boundaries, the second alignment offset from the first alignment relative to the burst boundaries, the offset sufficient to enable selection for retrieval of the data from the first alignment or the second alignment; and

decoding a frame with a video decoder using at least a portion of the data, wherein the data represents at least one reference frame.

2. (Cancelled)

3. (Currently Amended) The method of claim 1 ~~2~~ wherein the video decoder is an H.264 codec.

4. (Original) The method of claim 1 wherein the machine readable memory device comprises volatile memory.

5. (Original) The method of claim 4 wherein the volatile memory is one of static random access memory and dynamic random access memory.

6. (Original) The method of claim 1 wherein the machine readable memory device comprises non-volatile memory.

7. (Original) The method of claim 6 wherein the non-volatile memory is read-only memory.

8. (Original) The method of claim 1 further comprising storing the data in the machine readable memory device a third time at a third memory address, the third memory address having a third alignment with respect to the burst boundaries.

9. (Previously Presented) A method for use in managing bursts of data, the method comprising:

determining a set of desired bytes of data, the set of desired bytes of data having been previously stored in a machine readable memory device at two or more memory addresses, the memory device having at least two burst boundaries, and each memory address offset from the other memory address relative to the burst boundaries, the offset sufficient to enable selection for retrieval of the data from only one of the memory addresses; and

retrieving the desired bytes of data from a preferred memory address, the preferred memory address being aligned with the at least one burst boundary such that the number of bursts necessary to read the desired bytes from the preferred memory address is fewer than the number of bursts necessary to read the desired bytes from the other memory addresses; and

decoding a frame with a video decoder using at least a portion of the data, wherein the data represents at least one reference frame.

10. (Cancelled)

11. (Currently Amended) The method of claim 9 ~~10~~ wherein the video decoder is an h.264 codec.

12. (Original) The method of claim 9 wherein the machine readable memory device comprises volatile memory.

13. (Original) The method of claim 12 wherein the volatile memory is one of static random access memory and dynamic random access memory.

14. (Original) The method of claim 9 wherein the machine readable memory device comprises non-volatile memory.

15. (Original) The method of claim 14 wherein the non-volatile memory is read-only memory.

16. (Currently Amended) A circuit for ~~managing bursts of~~ decoding video data, the ~~method~~ circuit comprising:

a machine readable memory device, having two or more burst boundaries, for storing data starting at a first memory address that has a first alignment with respect to the burst boundaries, and concurrently storing the data starting at a second memory address that has a second alignment with respect to the burst boundaries, the second alignment offset from the first alignment relative to the

burst boundaries, the offset sufficient to enable selection for retrieval of the data from the first alignment or the second alignment; and

a circuit for writing the data to the machine readable memory device a first time starting at the first memory address that has the first alignment with respect to the burst boundaries and writing the data in the machine readable memory device a second time starting at the second memory address that has the second alignment with respect to the burst boundaries; and

a video decoder for decoding a frame at least a portion of the data, wherein the data represents at least one reference frame.

17. (Currently Amended) A circuit for ~~managing bursts of~~ decoding video data, said circuit comprising:

a machine readable memory device, having two or more burst boundaries, for storing data starting at a first memory address that has a first alignment with respect to burst boundaries, and concurrently storing the data starting at a second memory address that has a second alignment with respect to the burst boundaries, the second alignment offset from the first alignment relative to the burst boundaries, the offset sufficient to enable selection for retrieval of the data from the first alignment or the second alignment; and

a circuit for determining a first number of bursts for retrieving the data from the first address and determining a second number of bursts for retrieving the data from the second address and retrieving the data from the first address if the first number of bursts is fewer than the second number, and retrieving the data from the second

address if the second number of bursts is fewer than the first number; and

a video decoder for decoding a frame at least a portion of the data, wherein the data represents at least one reference frame.

18. (Cancelled)

19. (New) The method of claim 1, further comprising:

outputting the decoded frame.

20. (New) The method of claim 19, wherein outputting the decoded another frame comprises displaying the decoded frame.

21. (New) The method of claim 8, further comprising:

outputting the decoded frame.

22. (New) The method of claim 21, wherein outputting the decoded frame comprises displaying the decoded frame.

23. (New) The circuit of claim 16, further comprising:

outputting the decoded frame.

24. (New) The circuit of claim 23, wherein outputting the decoded frame comprises displaying the decoded frame.

25. (New) The circuit of claim 17, further comprising:

outputting the decoded frame.

26. (New) The circuit of claim 25, wherein outputting the decoded frame comprises displaying the decoded frame.